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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	09/421,217	TAKAHASHI, HIDEKI
	Examiner: Steven Loke	Art Unit: 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-39* is/are pending in the application.

4a) Of the above claim(s) *27-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 22 and 24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kumagi.

In regards to claim 22, Kumagi shows all the elements of the claimed invention in fig. 4. It is an insulated gate semiconductor device, comprises: a first semiconductor layer [61] of a first conductivity type (p) having first and second main surfaces on opposite sides thereof; a second semiconductor layer [63] of a second conductivity type (n) provided on the first main surface of the first semiconductor layer; a third semiconductor layer [64] of the second conductivity type higher in an impurity concentration (n+) and thinner than the second semiconductor layer [63], and provided on a surface of the second semiconductor layer [63]; a fourth semiconductor layer [55] of the first conductivity type provided on a surface of the third semiconductor layer [64], wherein the third semiconductor [64] is interposed between the second semiconductor layer [63] and a bottom of the fourth semiconductor layer [55] and is in direct contact with said second semiconductor layer [63]; a fifth semiconductor layer [56] of the second conductivity type selectively provided in a surface of the fourth semiconductor layer [55] and opposing the third semiconductor layer [64] through the fourth semiconductor layer [55]; a first main electrode [21] disposed across and connected with surfaces of the fourth and fifth semiconductor layers [55, 56]; a second main electrode [12] provided on

the second main surface of the first semiconductor layer [61]; an insulating film [57] provided on a portion of the fourth semiconductor layer [55] interposed between the third and fifth semiconductor layers [64, 56]; a control electrode [23] facing the portion through the insulating film [57] so that the portion forms a channel region.

In regards to claim 24, Kumagi discloses a sixth semiconductor layer [62] of the second conductivity type higher in an impurity concentration (n) than the second semiconductor layer [63] provided between the first and second semiconductor layers [61, 63].

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagi.

In regards to claim 23, it would have been obvious for the second semiconductor layer extends through the first semiconductor layer and is partially exposed in the second main surface of the first semiconductor layer because it depends to the switching speed of the device.

In regards to claim 25, it would have been obvious for the sixth semiconductor layer extends through the first semiconductor layer and is partially exposed in the second main surface of the first semiconductor layer because it depends to the switching speed of the device.

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 22 and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of U.S. Patent No. 5,751,024. Although the conflicting claims are not identical, they are not patentably distinct from each other because both of them disclose a semiconductor device comprising: a first semiconductor layer of a first conductivity type having first and second main surfaces on opposite sides thereof; a second semiconductor layer of a second conductivity type provided on the first main surface of the first semiconductor layer; a third semiconductor layer of the second conductivity type higher in an impurity concentration and thinner than the second semiconductor layer, and provided on a surface of the second semiconductor layer; a fourth semiconductor layer of the first conductivity type provided on a surface of the third semiconductor layer, wherein the third semiconductor is interposed between the second semiconductor layer and a bottom of the fourth semiconductor layer and is in direct contact with said second semiconductor layer; a fifth semiconductor layer of the second conductivity type

selectively provided in a surface of the fourth semiconductor layer and opposing the third semiconductor layer through the fourth semiconductor layer; a first main electrode disposed across and connected with surfaces of the fourth and fifth semiconductor layers; a second main electrode provided on the second main surface of the first semiconductor layer; an insulating film provided on a portion of the fourth semiconductor layer interposed between the third and fifth semiconductor layers; a control electrode facing the portion through the insulating film so that the portion forms a channel region; the first main electrode not contacting any other semiconductor layer than the fourth and fifth semiconductor layers.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
February 22, 2002

Steven Loke
Primary Examiner